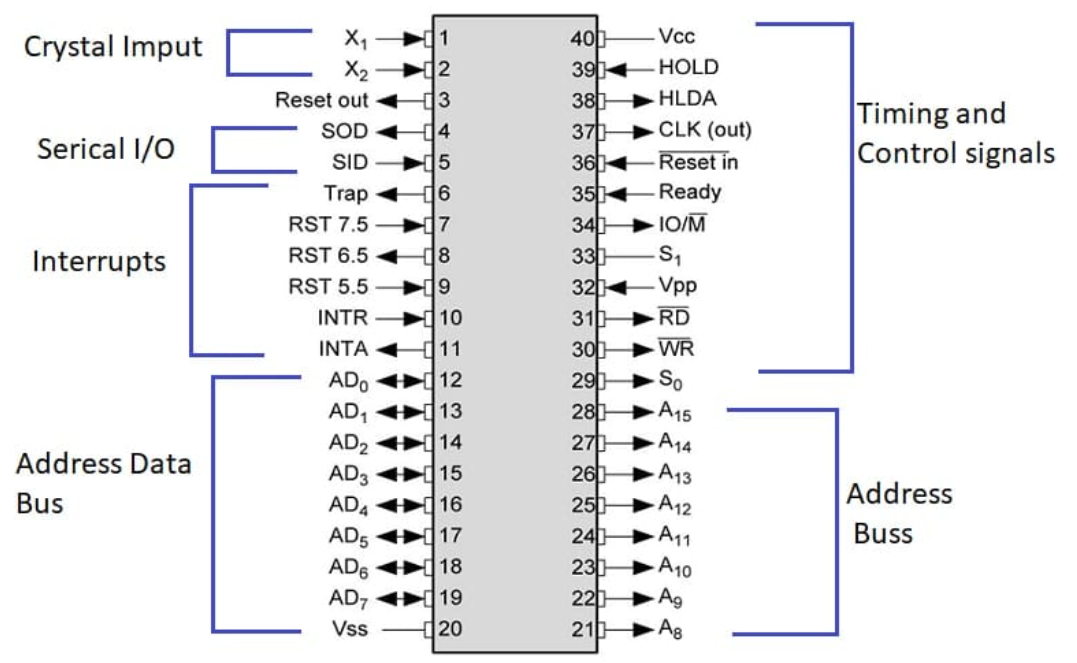
**8085 PIN DIAGRAM**



**Parts of 8085 Microprocessor**

* Crystal input
* Serial I/O
* Interrupts
* Address data bus
* Timing and control signals
* Address bus

**X1 and X2**

* Crystal oscillators.
* Provides **frequency** to the microprocessor.

**Address Bus**

* Makes **data transfer**.

**Address Data Bus**

* Called **multiplexing lines**.
* **Bidirectional** data transfer.

**ALE**

* Address latch enable.
* Enables the **address bus**.

**IO/M**

* Status signal.
* Tells whether address is for **memory** or **I/O**.
* **Positive** signal means **I/O read** or **I/O write**.
* **Negative** signal means **memory activation**.

**S0 or S1**

* Status signals.
* **00** means **HALT** operation.
* **01** means **READ** operation.
* **10** means **WRITE** operation.
* **11** means **FETCH** operation.

**RD**

* Low energetic pin.

**WR**

* Writes data to **peripherals** and/or **memory**.

**Ready**

* **Decides** whether the device will **receive** or **transmit** **data**.
* High pin means device is **ready** for transfer.
* Else **not**.

**HOLD**

* Tells if a device needs to use both **A** and **AD** bus.

**HLDA**

* Detects whether **HOLD** is receiving signals or **not**.
* Goes **low** immediately after giving response.

**INTR**

* **Lowest** **priority** interrupt signal.

**INTA**

* Interrupt acknowledgement.
* Recognises interrupt signals.
* **Active-low** signal (processes for 0 only & not 1).

**RST**

* Restart maskable interrupts.
* Also called **vectored interrupts**.

**TRAP**

* **Non-maskable** interrupt (**doesn’t** stops the program).
* Interrupt precedence order: **TRAP** > **RST 5.5** > **RST 6.5** > **RST 7.5** > **INTR**

**RESET IN**

* **Resets** program counter to **zero**.
* Rearranges **interrupt enable** & **HLDA** flip-flops.

**RST OUT**

* Resets all the devices connected to microprocessor.

**CLK**

* Generates clock signals for peripherals etc.

**SID and SOD**

* Used for serial data communication.
* Verifies if interrupt is covered or not.

**Vss and Vcc**

* Vss is a **ground** pin.
* Vcc is a **+5v** pin.

**TIME DIAGRAM**

**Size Distribution**

* An **opcode** (**mnemonic**) is of **1 byte**.
* Also the mentioned address is of **1 byte**.
* The **address data** is stored **next to opcode** data in memory.
* **Program counte**r (PC) points to the **first address** and increments by one to point next address.
* **High impedance state:** A pin is not working currently.

**Graph Elements Analysis**

* **ALE**
  + Signal **0** means **data** is travelling through bus.
  + Signal **1** means **address**…
* **IO/M**
  + Signal **0** means we are working with **memory**.
  + Signal **1** means … **I/O devices**.
* **S0 and S1**
  + If **S0=0** and **S1=1** then our processor is **performing write operation**.
  + If **S0=1** and **S1=0** then our processor is **performing read operation**.
  + If **S0=1** and **S1=1** then our processor is **fetching opcode**.
* **RD**
  + **0** means we can now **read** data.

**Examples**

* IO/M=0 and S0=1 and S1=1 means we are **fetching opcode from memory**.
* IO/M=1 and S0=0 and S1=1 means we are **reading from I/O device**.

**Workings**

* **Program counter** tells on what we are working on by **pointing** it.
* **IO/M** and **S0** and **S1** pins are drawn together on graph as single unit.
* Address of **4-digits** are broken into **two parts**.
* For example, **2051H** is broken into **20H** and **51H**.
* **Address bus** carries **20H** and **address/data bus** carries **51H**.
* **MVI A** is stored as value **3E**.
* Opcode is **fetched first**, then it is **decoded**.

**The Diagram**

